

**IN THE CLAIMS**

Claim 1 (Currently Amended): A semiconductor device, comprising:

a first interconnect layer disposed over a substrate where a functional semiconductor region is formed;

an inter layer dielectric directly covering a portion of top surface and side surfaces of said first interconnect layer;

[[;]]

a silicon nitride film formed so as to cover entirely a top surface of said inter layer dielectric;

a metal interconnect layer covering said silicon nitride film, said metal interconnect layer being consisted of gold material, ~~wherein said metal interconnect layer is an uppermost interconnect layer having a thickness capable of protecting the first interconnect layer and a device region of the semiconductor device; and~~

a planarized polyimide which is formed directly on a surface of the silicon nitride film and directly surrounding the metal interconnect layer including a side wall thereof,

wherein a portion of the planarized polyimide is removed at a part of a region of the metal interconnect layer and a bonding wire is connected to the region of the metal interconnect layer.

Claim 2 (Canceled).

Claim 3 (Previously Presented): A semiconductor device according to claim 1, wherein said silicon nitride film is formed by high-density plasma CVD method.

Claim 4 (Canceled).

Claim 5 (Withdrawn): A method for manufacturing a semiconductor device comprising steps of:

a process for forming a foundation interconnect layer on a surface of a semiconductor substrate on which a functional semiconductor region is formed;

a process for forming an inter layer dielectric on said foundation interconnect layer of which surface is shaped as convex and concave shape;

a process for forming silicon nitride film on said inter layer dielectric;

a process for forming metal interconnect layer as an uppermost layer interconnects an upper layer of said silicon nitride film, said metal interconnect layer being consisted of gold; and

a process for coating a polyimide resin film on said metal interconnect layer and planarizing surface thereof.

Claim 6 (Withdrawn): A method for manufacturing a semiconductor device according to claim 5, wherein said metal interconnect layer is connected to said foundation interconnect layer through a through hole formed in-between thereof and further wherein said interconnect layer is low in resistance and formed thicker than thickness of said foundation interconnect layer.

Claim 7 (Withdrawn): A method for manufacturing a semiconductor device according to claim 6, wherein said method further includes a process for removing a part of region of said polyimide resin layer, and a process for wire-bonding at said part of region so as to connect to a surface of said metal interconnect layer.

Claim 8 (Currently Amended): A semiconductor device, comprising:

a first interconnect layer covering a first portion of a surface of a functional semiconductor region;

an inter layer dielectric covering a second portion of the surface of the functional semiconductor region and directly covering a portion of top surface and side surfaces ~~portion of a surface of~~ said first interconnect layer, thereby defining ~~forming~~ a contacting hole on the surface of the first interconnect layer;

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a silicon nitride film covering an entire top surface of said inter layer dielectric around the contacting hole on the surface of the first interconnect layer;

a barrier layer covering the contacting hole and a portion of a surface of the silicon nitride film around the contacting hole, thereby forming a barrier layer region;

a metal interconnect layer consisting of gold material covering the barrier layer region, thereby forming a metal interconnect region, ~~wherein said metal interconnect layer is a uppermost interconnect layer having a thickness capable of protecting the first interconnect layer and a device region of the semiconductor device;~~ and

a planarized polyimide which is formed directly on a surface of the silicon nitride film and directly surrounding the metal interconnect layer including a side wall thereof,

wherein a portion of the planarized polyimide is removed at a part of a region of the metal interconnect layer and a bonding wire is connected to the region of the metal interconnect layer.

Claim 9 (Previously Presented): The semiconductor device of claim 8, wherein the barrier layer consists of titanium.

Claim 10 (Previously Presented): The semiconductor device of claim 9, wherein the first interconnect layer consists of aluminum.

Claim 11 (Previously Presented): The semiconductor device of claim 8, wherein the first interconnect layer consists of aluminum.

Claim 12 (Previously Presented): The semiconductor device of claim 8, wherein the inter layer dielectric consists of USG film.

Claim 13 (Previously Presented): The semiconductor device of claim 8, wherein the functional semiconductor region further comprises a polysilicon gate isolated from the first interconnect layer by a third dielectric layer, wherein the first interconnect layer is connected to the polysilicon gate through a contacting area disposed within the third dielectric layer.